Invited Paper

Devices and architectures for large scale integrated silicon photonics circuits

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ABSTRACT

We present DWDM nanophotonics architectures based on microring resonator modulators and detectors. We focus on two implementations: an on chip interconnect for multicore processor (Corona) and a high radix network switch (HyperX). Based on the requirements of these applications we discuss the key constraints on the photonic circuits' devices and fabrication techniques as well as strategies to improve their performance.

Keywords: Silicon photonics, microring resonators, nanophotonics architectures

1. INTRODUCTION

Silicon photonics, with its promise of large scale integration and low cost, is poised to revolutionize data links at scales ranging from the chip to the datacenter. Many groups have introduced dense wavelength division multiplexing (DWDM) nanophotonics architectures based on silicon photonic. Here we focus in particular two architectures based on microring resonator modulators and detectors: an on-chip interconnect for a many-core processor (Corona[1,2]) and a high-radix photonic switch for an exascale datacenter network (HyperX[3]). The stringent requirements that these applications place on the photonic circuit performance require a careful optimization of the devices' design and fabrication strategies of large scale integrated circuits. The key technological constraints stem from the need to use DWDM to fulfill bandwidth requirements. DWDM requires modulation, multiplexing, and demultiplexing of sources with closely spaced frequencies. Ring resonators are well suited for DWDM applications but present a series of challenges because the difficulties in controlling their performance parameters such as the resonant frequency, quality factor, and extinction ratio. For example, while it is possible to actively control the resonant frequency (e.g. by temperature tuning) the amount of tuning necessary has a large impact of the system power consumption. Fabrication parameters also affect other properties of the rings such as the extinction ratio that have a large impact on the design of the integrated electronic-photonic circuit. Here we summarize our efforts to study the effect of fabrication variations on the ring parameters and the effect of these variations on system performance as well as ways to mitigate these effects.

2. PHOTONIC-ENABLED ARCHITECTURES

The first architecture we consider here has been discussed in detail in a paper by Vantrease *et al.*[1] as well as by Ahn *et al.*[2] Figure 1 shows a schematic of the Corona architecture. Corona is a many-core chip in which cores are clustered in groups comprising 4 cores that share L2 cash as well as other infrastructure such as memory controllers and network interfaces. The clusters are interconnected by an optical crossbar that uses DWDM to increase bandwidth density. The photonic links use a multiple-sender single-receiver architecture that allows us to create a complete crossbar (a network in which each node can directly communicate o any other node without intermediate hops) with a relatively small number of devices and waveguides. Thanks to this topology we have shown that Corona can outperform all-electrical counterparts.[1]

In addition to the internal crossbar Corona has photonic connection to external Optically Connected Memories (OCMs). Using these external connections a Corona chip can be used as a switch with a large number of ports. This is shown schematically in Fig. 2. In this implementation much of the compute power has been eliminated and the whole chip is used just to direct incoming packets from an input port to an output port. The advantage of

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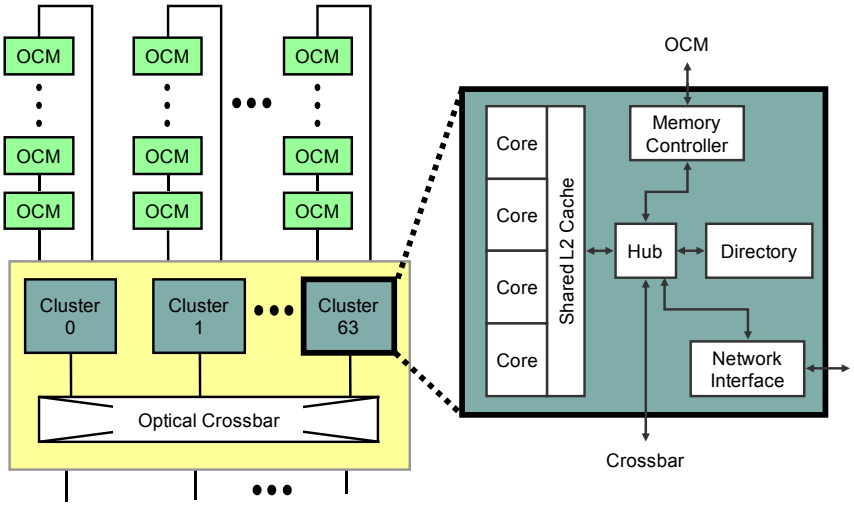

Figure 1. Schematic view of the Corona architecture.[1] OCM: optically connected memory.

this approach is that it allows us to build networks with high connectivity.[3] For example Ahn *et al.*[3] have shown that using 128 port switches it is possible to build a network with 64,000 nodes (i.e. an exaflop supercomputer) in which each node is at most 4 hops away from any other node on the network.

Both these implementations rely heavily on photonics interconnects and exploit their advantages. The most evident advantage of an on-chip interconnect is the ability to increase the bandwidth density by the use of DWDM. A second advantage is the lower energy per bit that photonic interconnects are expected to achieve compared to their electrical counterparts. The relative insensitivity of photonic interconnects to electro magnetic interference is also an important factor. In addition to these well known advantages we have found out that computer-com photonics network have architectural advantages that are less well understood. For example, because the waveguide loss is relatively small compared with the power necessary to modulate and detect light, the main power consumption of a photonic link happens at the terminals. This allows us to build large networks that are relatively insensitive to distance: one can build links with a wide range of length. This allows one to build flat architectures that are less hierarchical and therefore easier to program and manage. Also a crossbar like the one described in Corona[1] enabled by multiple-sender single-receiver links is a key element that allows large, highly interconnected networks to be built on-chip using a relatively small number of waveguides and other photonic devices. Electronic networks with comparable connectivity would be impractical and very hard, if not impossible, to build.

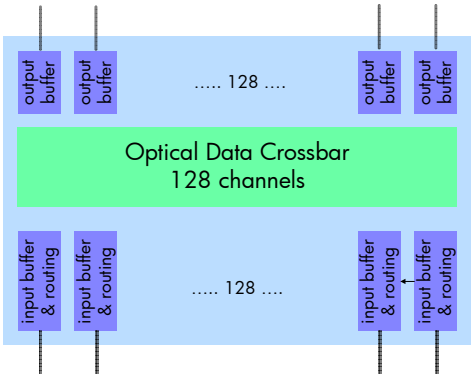

Figure 2. Schematic of a high-radix photonic switch[3]

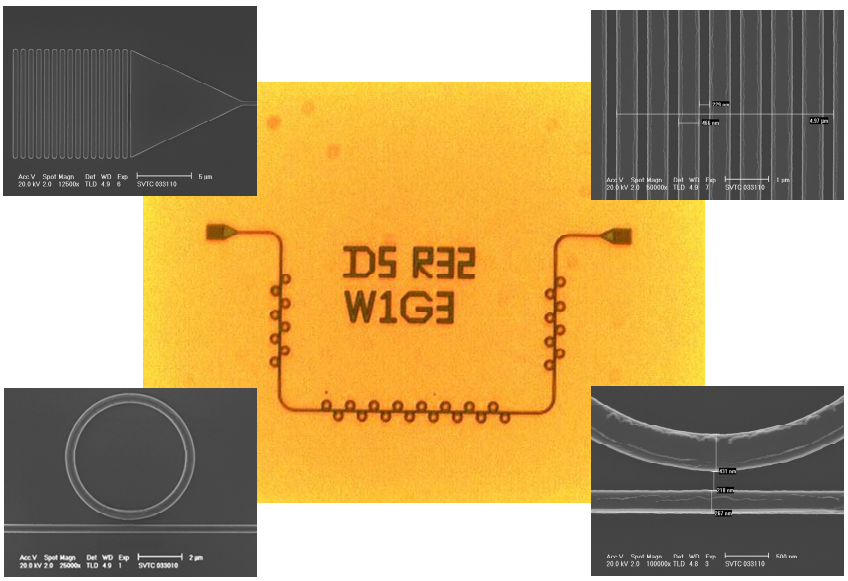

Figure 3. Photonic interconnect devices fabricated using DUV lithography on SOI substrates

3. SILICON PHOTONIC DEVICES

To implement the photonic enabled architectures described in the previous section one needs a DWDM network. The substrate of choice for our devices is silicon on insulator because it allows us to leverage the existing CMOS fabrication technology. We chose to use ring resonators because they work in an intrinsically DWDM. Microring resonators can be used as modulators for on-off keying[4] and as narrowband drop-off filters for demultiplexing DWDM signals. Germanium can be integrated in CMOS technology to build efficient detectors.[5] The main disadvantage of the ring resonators is that the resonant frequency and other key performance parameters are very sensitive to fabrication variations as well as environmental changes. Here we study these effects on devices fabricated using a standard CMOS fabrication facility.

The devices were fabricated using a standard 248-nm 8 inch photolithography process in an external foundry. The process starts with a SOI wafer that has a 250-nm silicon layer sitting on top of 3 μm layer of silicon oxide. The photolithography masks has a target critical dimension (CD) of 200 nm and a CD tolerance of $\pm$15 nm. The design is locked to a 20 nm grid that corresponds to a 5 nm grid on the silicon wafer when the 4x reduction of the stepper is taken into account. We define 450 nm-wide rings with nominal diameters of 10 μm, 5 μm, and 3 μm. The rings are placed next to straight bus waveguides. In some of the devices on the die the distance between the waveguide and the ring as well as the bus waveguide width is changed to allow us to optimize coupling and minimize losses.[6] The waveguides are etched to a nominal depth of 200 nm and a 50 nm silicon layer is preserved to allow charge injection through a lateral p-i-n structure in future devices. Each die contains approximately 1500 devices and thousands of microrings. The devices were designed to study various components and parameter variations. Figure 3 shows picture of the fabricated devices. Coupling in and out of the bus waveguide can is achieved through grating couplers (detail shown in the upper left SEM image) thus allowing wafer-level testing without need to dice and polish the devices. At the time of writing we are processing a batch of active devices that include full modulators and thermal controls to tune the resonant frequency of the rings. We are also working to include detectors in our fabrication process.

Figure 4 shows the transmission curves for microring resonators of three different diameters: 10 μm, 5 μm, and 3 μm. We designed our chip to have multiple versions of these resonators with varying gaps between the ring and the bus waveguide, as well as varying the width of the bus waveguide. In what follows, we concentrate on results

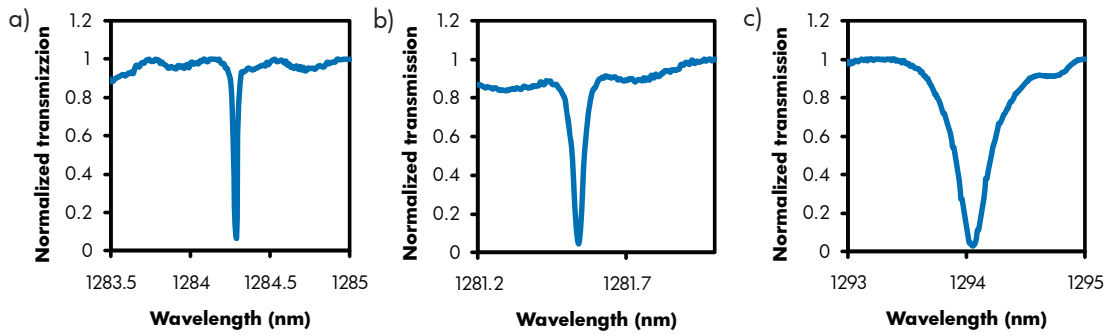

Figure 4. Normalized transmission curves for critically coupled rings of various diameters: (a) 10 μm, (b) 5 μm, and (c) 3 μm.

Table 1. Summary of critically coupled devices' properties.

Diameter	10 μm	5 μm	3 μm
Q	60,000	34,000	3,400
WG width	350 nm	300 nm	300 nm
Gap	250 nm	300 nm	200 nm

for the resonators that are closest to critical coupling, summarized in Table 1. Notice that the quality factor of the rings is dramatically affected by the ring diameter, in that smaller rings have increased bending losses. Since their quality factors are so high, we conclude that for 10-μm diameter rings the losses are dominated by scattering losses due to surface roughness. In the 5-μm rings the scattering and bending losses are approximately equal and therefore we see a reduction of the quality factor by 1/2 compared with the 10-μm results. The 3-μm rings are dominated by bending losses and in particular by the losses introduced by the 50-nm pedestal used to inject current in the finished modulators. These results are in qualitative agreement with our numerical simulations.

We study the effects of SOI wafer properties and fabrication variations on microring performance characteristics. Using a Cascade-Microtech Summit 12000 automated probe station specially fitted for photonic wafer-level

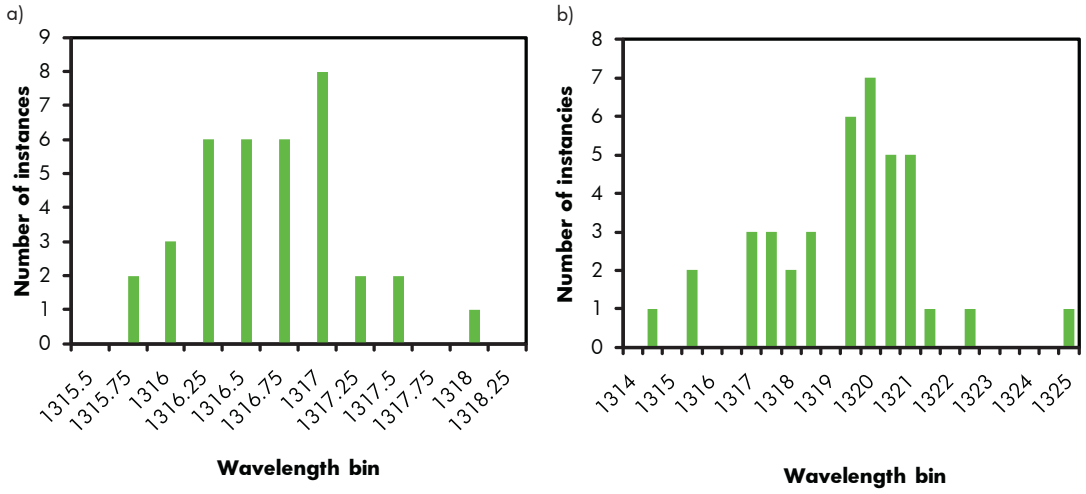

Figure 5. Effect of fabrication variations on the wavelength of nominally identical 10 μm rings (a) across a die and (b) across an 8" wafer.

testing, we analyzed the ring performance cross-die and cross-wafer. Figure 5 shows a comparison of the variation in the ring's resonant wavelength measured (a) across a die and (b) across a chip. A statistical analysis of this data shows that across the die the variance is $\sigma_D = 0.5$ nm, while across the wafer the variance is $\sigma_W = 2.0$ nm, indicating that this effect is caused by variations of the process across the wafer. There are two possible causes for this result: variations in the silicon layer thickness, and variations in the etch depth. According to the SOI manufacturer the top Si layer thickness for our wafers is 250 ± 12.5 nm (mean + 3σ), while according to the external fab the etch depth is 200 ± 10 nm (mean + 3σ). We used a finite element analysis program to simulate the effect of these variations on the resonant frequency of a 10 μm-diameter microring, and we have plotted the results shown in Fig. 6. We note that large variations of the resonant frequency can occur within the 6σ fabrication tolerances, methods to mitigate these effects need to be developed. An understanding of fabrication variations and their effect on the performance of photonic devices is a key element that would allow us to design and optimize photonic-enabled architectures like those presented in Section 2.

Precise definition of the rings' resonant frequencies has a very large impact on the architecture and power consumption of DWDM systems based on ring modulators. Rings that have a resonant frequency different from that of the design will need to be brought into compliance. In our DWDM feasibility studies we assumed that heating the rings can be used to bring them into compliance thus adding to the power consumption and thermal load of an on-chip DWDM system. Initial unoptimized experiments carried out in our lab show that 5 mW/nm are necessary to thermally tune microring resonators like the ones we use here. Similar results were obtained by other groups.[7] This would imply that with the technology used here each ring would need to be thermally tuned, on average, by 6 nm (using a 6σ tolerance) to compensate the effects of cross-wafer wavelength scattering. The associated power cost of 30 mW per ring would add considerable power and thermal load to a chip. Further investigation is needed to determine the causes of the frequency scatter and chart possible routes to improvement.

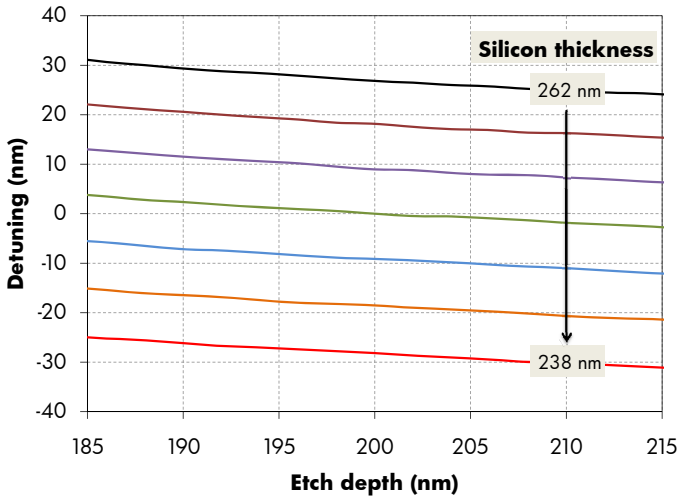

Figure 6. Calculated wavelength shift for 10 μm ring resonators, where we have varied the initial thickness of the silicon layer and the etch depth.

4. CONCLUSIONS

We have presented a short overview of key photonic-enabled architectures and the photonic technologies needed to build them. We believe that the use of DWDM photonic devices will bring an increase in the bandwidth density and a decrease in power consumption for computer-com applications. In addition photonic networks enable the deployment of radically new architectures. These architectures will allow one to build systems that are larger and more powerful than their electrical counterparts but also, because of their better connectivity, simpler to program and manage.

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